High-speed and high-power semiconductor material advances

Mike Cooke reports on the wide spectrum of compound semiconductor advances reported at December's International Electron Devices Meeting in San Francisco.

At the International Electron Devices Meeting (IEDM 2018) in San Francisco (1–5 December), there were two main threads in the compound semiconductor contributions — high-speed and high-power devices. The first, speed aspect in general looks to narrow-bandgap materials, since these tend to have smaller effective masses of charge carriers and hence a higher-mobility response to the force supplied by electric fields. The second, power strand needs the ability to withstand high electric fields and voltage blocking, enabled by wide bandgaps, while maintaining low resistance in the on-state.

IEDM has contained presentations on compound semiconductor electronics with these aims for a number of years. While initially it was thought that high-speed, narrow-bandgap materials might replace the more traditional silicon and silicon germanium (SiGe) even for logic applications, the focus now seems more on working out ways for compound semiconductor radio-frequency devices to be combined with more conventional group IV materials (silicon, germanium, tin) providing the digital processing.

On the power side, there is a wider range of choices, and the question is finding the right materials and structures for particular applications to enhance the capabilities already on offer by silicon and such. An aspect that seemed missing this year from the wide-bandgap considerations was combined high-speed and high-power for radio transmission amplifiers for base-station and radar use.

Here we look at how these strands have been pushed forward in the research presented at IEDM.

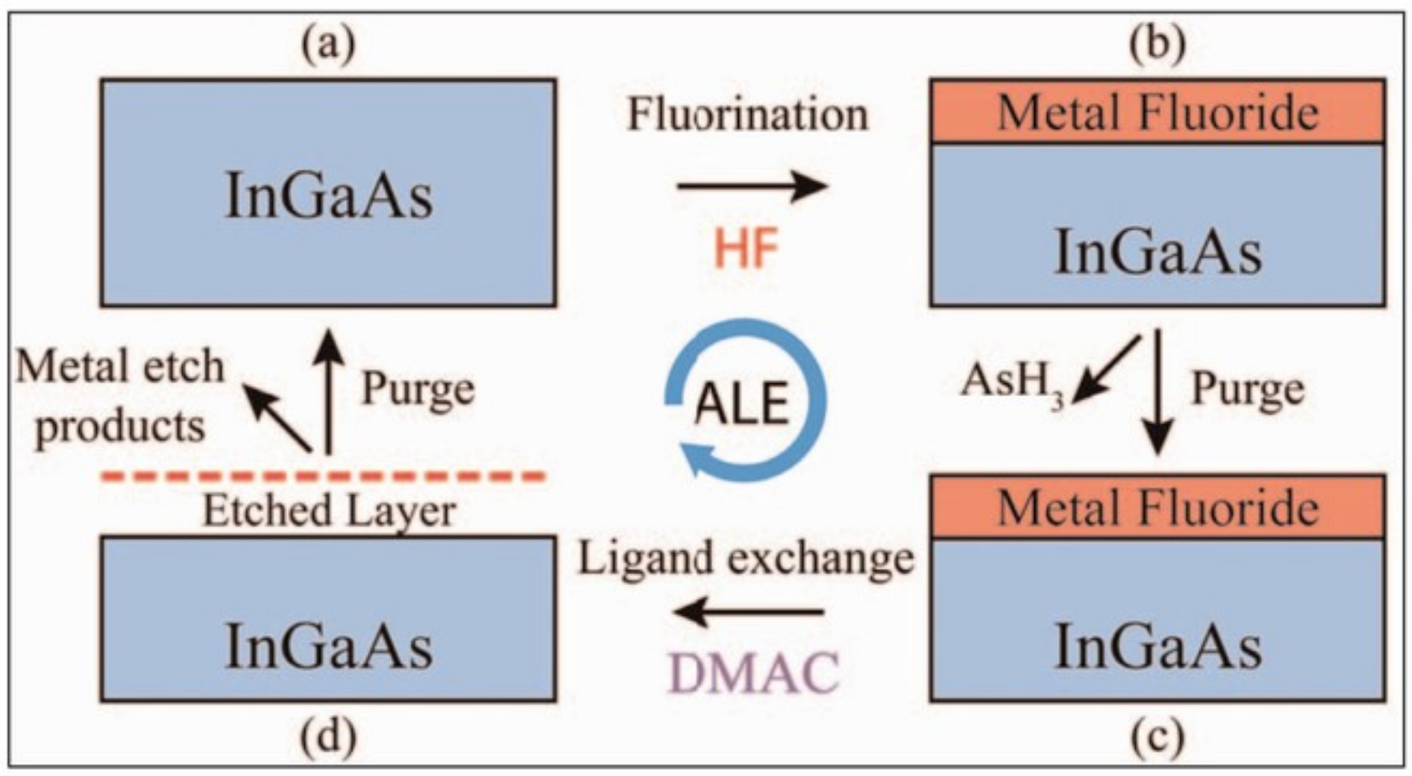

Figure 1. Schematic of InGaAs thermal ALE process: (a)–(b) fluorination of InGaAs surface with hydrogen fluoride, (c)–(d) ligand-exchange process by dimethylaluminum chloride to remove metal fluoride layer. Volatile etch products finally purged away.

High-speed performance

Fin structures

Massachusetts Institute of Technology and University of Colorado claimed the first demonstration of thermal atomic layer etching (ALE) of indium gallium arsenide (InGaAs)-based III–V heterostructures to create fin-gate transistors [Session 39.1]. "Also, we report the first transistors fabricated by the thermal ALE technique in any semiconductor system," the team adds.

The ALE technique was carried out in-situ in an atomic layer deposition (ALD) system at 300°C. The researchers used the method to fabricate sub-5nm self-aligned fin field-effect transistors (FinFETs), claimed as the "most aggressively scaled" so far. Fins with widths down to 2.5nm were fabricated.

A number of record results in terms of peak transconductance (g_m) and subthreshold swing were achieved with 60nm gate-length (L_g) devices. The average transconductance boost was 60% — the researchers achieved 0.85mS/μm with 2.5nm-wide fins (W_f) and 1.9mS/μm for 18nm at 0.5V drain bias. The average subthreshold swing was 70mV/decade in the linear (S_{lin}) region, and 74mV/decade in saturation (S_{sat}).

The researchers attribute the improvements to high-quality metal-oxide-semiconductor (MOS) interfaces arising from the use of in-situ ALE–ALD, with ALE used for fin etching and ALD for applying the aluminium oxide or hafnium dioxide gate insulation.

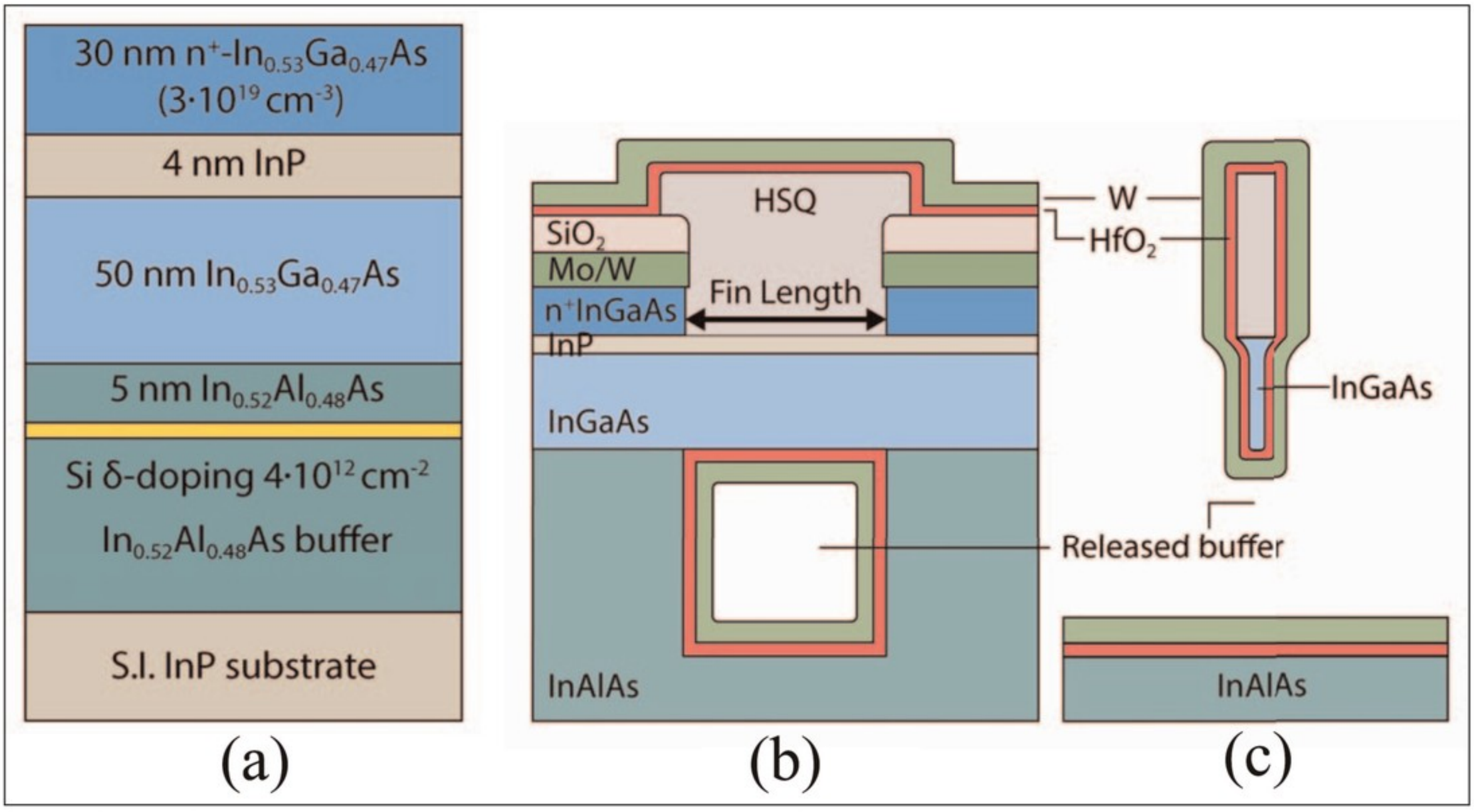

Figure 2. (a) Starting heterostructure for InGaAs n-channel FinFET fabrication. Cross-section schematics: (b) along fin length direction and (c) across fin.

The tungsten metal gate electrode was deposited in a separate ALD chamber.

Like ALD, thermal ALE is based on chemical ligand-exchange, enabling isotropic etch (Figure 1). For the thinnest finned FETs the structures were fully suspended from the buffer layer, resulting in gate-all-around structures (Figure 2).

The researchers comment: "With the usual caveats when making comparisons of this kind, our InGaAs FinFETs match the performance of Intel's 14nm node (W_f = 7nm), in spite of the lower V_{DD} and longer L_g. At W_f = 2.5nm, this work shows a record g_m/W_f > 30mS/μm. Given that this is the first demonstration of III–V MOSFETs by ALE and the first demonstration of working III–V FinFETs at W_f < 5nm, this work displays the great promise for both ALE technology and III–V devices."

Another series of record claims came from IBM Research Zurich and ETH Zurich in Switzerland [Session 39.2] for InGaAs-on-insulator on silicon FinFETs (Figure 3).

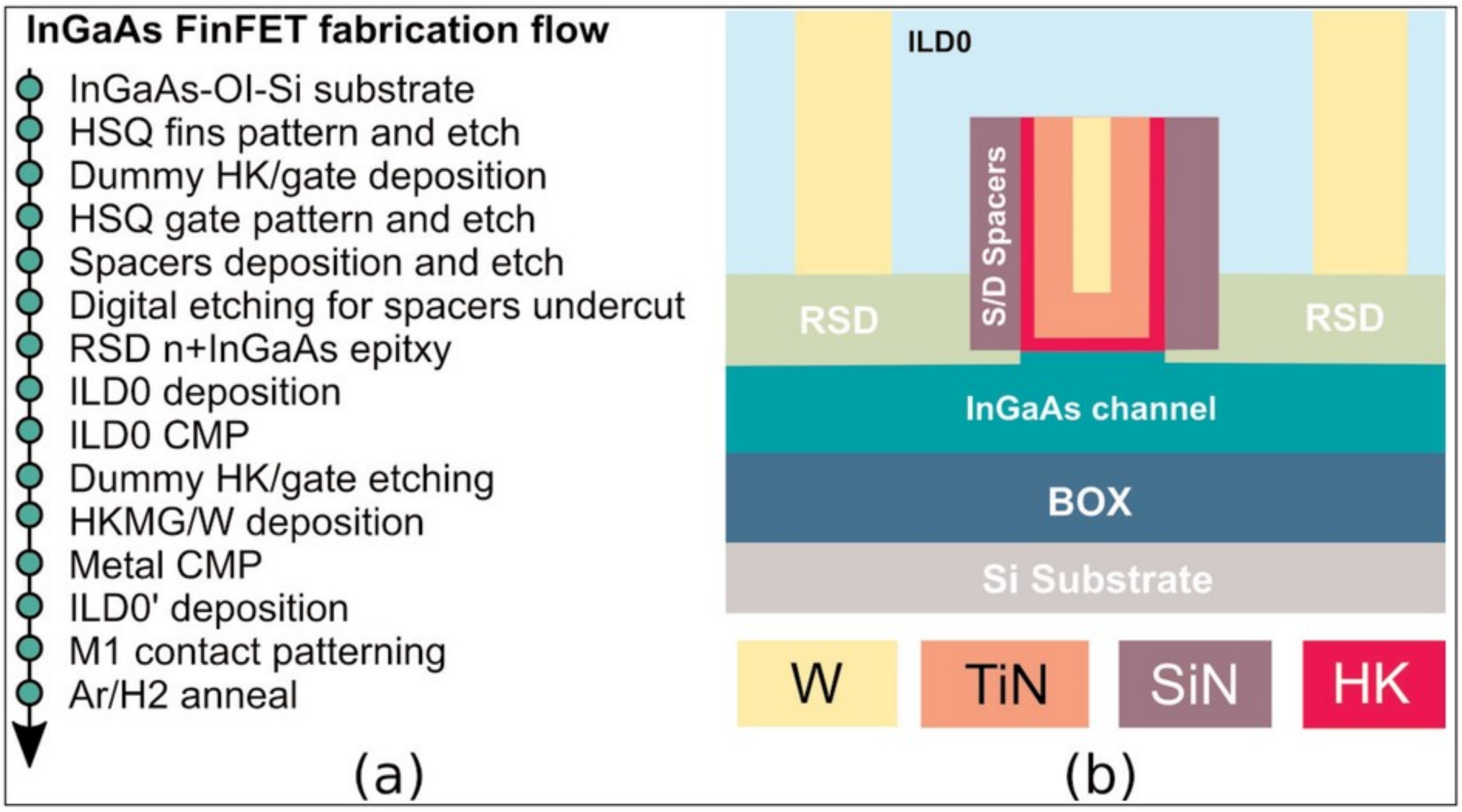

Figure 3. (a) Process flow describing self-aligned replacement-metal gate fabrication process for InGaAs FinFETs. (b) Schematic cross-section across gate.

The researchers used source/drain spacers and doped extensions to tamp down off-currents, which is difficult to suppress in narrow-bandgap high-mobility materials like InGaAs.

Devices with 20nm L_g, 10nm spacers and 15nm W_f achieved record high on-currents of 350μA/μm and off-current of 100nA/μm with 0.5V operation voltage (V_{sat}). The S_{sat} was 78mV/decade. The g_m was 1.5mS/μm. The InGaAs on buried oxide (BOX) insulator on silicon substrate was created by direct wafer bonding. The InGaAs channel layer was 20nm thick. The doped raised source/drain (R_{SD}) InGaAs contacts were 25nm thick.

MOS and CMOS

IBM Research GmbH Zürich Laboratory in Switzerland also claimed the highest reported combined cut-off and maximum oscillation frequencies (f_T/f_{max} of 370/310GHz) for III–V MOSFETs on silicon with 20nm gates [Session 39.4]. The InGaAs quantum well on silicon devices had gate lengths as short as 14nm. The replacement-metal gate fabrication process is said to be compatible with silicon CMOS processing, raising hopes for combining RF and digital signal processing on a single chip.

Again, spacers and self-aligned raised source/drain contacts are seen as significant enablers of enhanced performance. Also, channel mobility was increased three-fold using a 2nm/10nm/20nm InP/$In_{0.75}Ga_{0.25}As$/InP quantum well structure, relative to devices without the 2nm top barrier. The increased mobility was also reflected in 60% increased g_m. The InP/InGaAs/InP structures were transferred to silicon by direct wafer bonding.

IBM Research GmbH Zürich Laboratory further contributed to research at IBM T. J. Watson Research Center in the USA on a sub-50nm III–V FET on silicon with the highest on-current, according to the presentation [Session 39.5]. The device was a gate-all-around nanosheet InGaAs NFET grown using template-assisted selective epitaxy. The fabrication used a gate-last process and annealing in high-pressure deuterium. The latest work has managed to reduce the channel thickness to ~10nm. The best device had a 39nm L_g, giving 1.37mS/μm g_m, 72mV/decade S_{sat}, and 355μA/μm on-current at 0.5V gate potential and 0.5V drain bias.

The template-assisted selective epitaxy used metal-organic chemical vapor deposition (MOCVD) to grow III–V nanosheets from a silicon seed in a silicon dioxide tunnel mold on silicon-on-insulator (SOI) substrate (Figure 4). The gallium content of the InGaAs varied between 60% at the seed down to 40% at the end of the tunnel. The mold is formed by etching a 20nm-thick, 45nm-wide silicon nanosheet from the SOI material and enclosing it in oxide. The silicon nanosheet is then etched down to the seed from the other end of the tunnel structure.

Lund University in Sweden reported III–V MOSFET co-integration of n-type and p-type devices based on indium arsenide (InAs) and gallium antimonide (GaSb) channels, respectively [Session 39.3]. The self-aligned gate-last vertical nanowire devices achieved a balanced

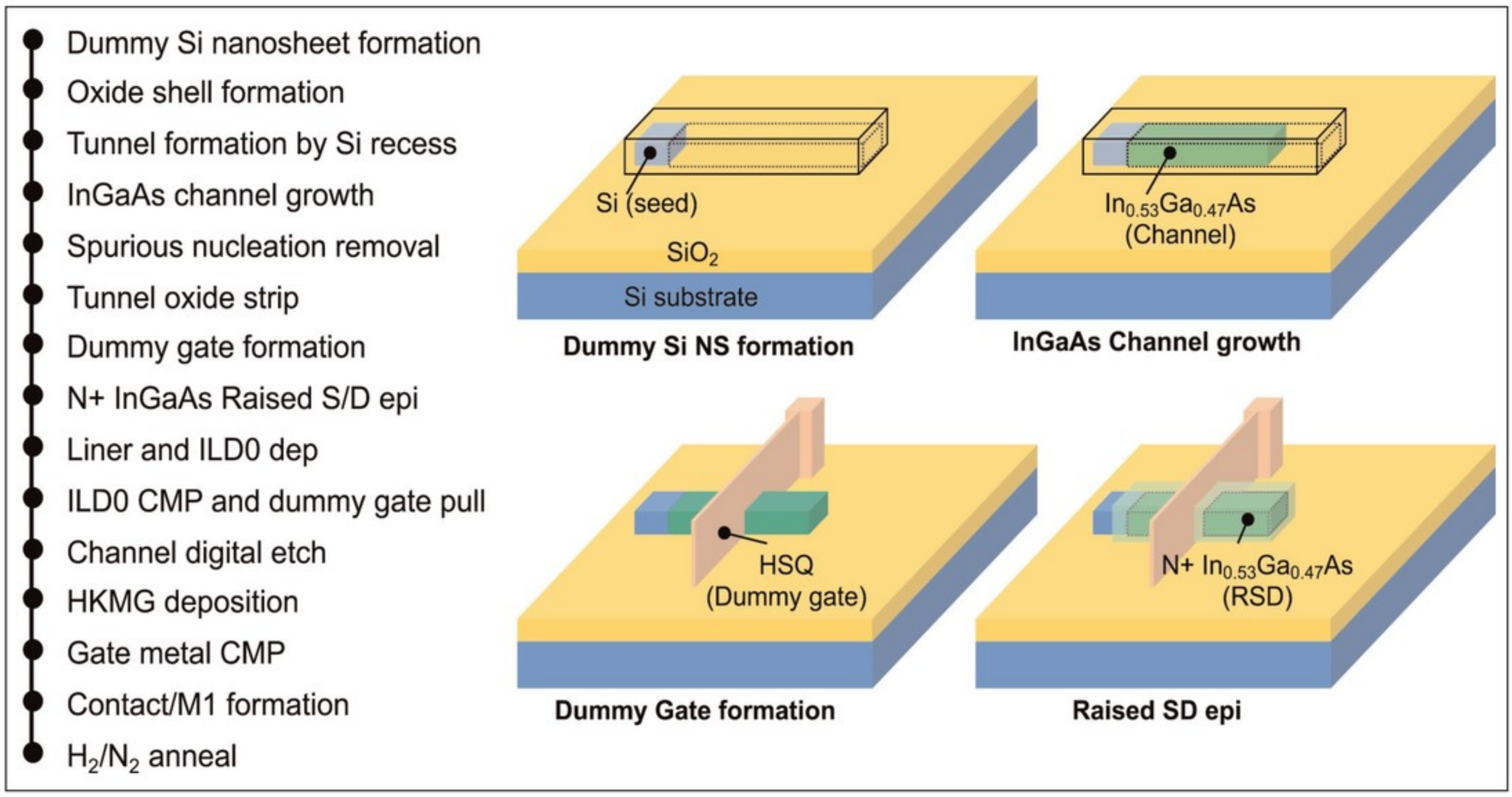

Figure 4. (left) Outline process flow of InGaAs nanosheet N-FET. (right) Schematics of process flow for nanosheet channel and raised S/D formation.

drive current at the 100μA/μm level. The off-current was 100nA/μm with the drain biased at 0.5V.

Tunneling and negative capacitance

Switzerland's EPFL, Belgium's imec and Japan's Tokyo Institute of Technology claimed the first experiments demonstrating the benefits of negative capacitance (NC) on the performance of tunneling FETs (TFETs) [Session 13.4]. Quantum mechanical band-to-band tunneling, as opposed to the thermionic injection of conventional MOSFETs, enables sub-thermionic sub-threshold-swing values (i.e. less than 60mV/decade).

The devices connected ferroelectric negative capacitors to the gate of InGaAs TFETs. The negative capacitance was chosen so that, combined with the gate capacitance, a positive value was maintained for stability over the operation range (Figure 5).

The ferroelectric used was single-crystal lead zirconate titanate ($Pb(Zr,Ti)O_3$, or PZT). The material for the negative capacitor was grown by pulsed laser deposition — the substrate was dysprosium scandium oxide ($DyScO_3$) substrate with 20nm strontium rubidium oxide ($SrRuO_3$, or SRO) bottom electrode and 46nm PZT. The top electrode was 50nm sputtered platinum.

The TFETs were homojunction devices using $In_{0.53}Ga_{0.47}As$ MOCVD material on InP substrate. The gate stack consisted of 1nm Al_2O_3 and 2nm HfO_2 insulation, and 100nm titanium nitride (TiN) as metal electrode. The TiN, diffusion doped with zinc, was also used for the source electrode.

The subthreshold swing (SS) of the TFET was as low as 55mV/decade, just below the thermionic level of 60mV/decade. The combination with 15μmx15μm negative capacitors enabled reduction of the SS to 30mV/decade, but with some hysteresis (~30mV in the threshold voltage between different sweeps). Reducing the area of the PZT negative capacitor to 10μmx10μm enabled sub-10mV hysteresis, along with a subthreshold swing as low as 40mV/decade.

The researchers see negative capacitance structures as being a "universal performance booster of FETs, significantly improving the SS and overdrive". In fact, the overdrive improvement enabled 50%-reduced supply voltages of 0.3–0.4V and lower power consumption.

Power performance

Gallium oxide

Gallium oxide (Ga_2O_3) has a wide bandgap of ~4.5eV, giving a high expected critical breakdown field of 8MV/cm. Electron mobility is a reasonable 200cm²/V-s. Melt growth methods have resulted in Ga_2O_3 substrates that are commercially available in circular (up to 2-inch diameter and more?) and rectangular formats (e.g. 10mmx15mm). On the negative side, there are concerns arising from the low thermal conductivity that self-heating effects could be a problem.

Cornell University in the USA, Kyoto University and Novel Crystal Technology Inc in Japan claimed the highest breakdown voltage and DC/pulsed Baliga figures of merit achieved so far for β-Ga_2O_3-based power devices [Session 8.5]. The reported vertical trench Schottky barrier diodes (SBDs) also managed to keep the reverse leakage current density below 1μA/cm² up to breakdown.

The researchers used halide vapor phase epitaxy (HVPE) to create a 10μm lightly doped n^--Ga_2O_3 drift layer on an n-type Ga_2O_3 substrate (Figure 6).

Device fabrication involved plasma etching trenches to a depth of the 1.55μm, giving a series of fins. A wet acid treatment was used to remove etch damage. The dry/wet etching resulted in rounded corners at the trench bottoms, which is favorable for reducing field

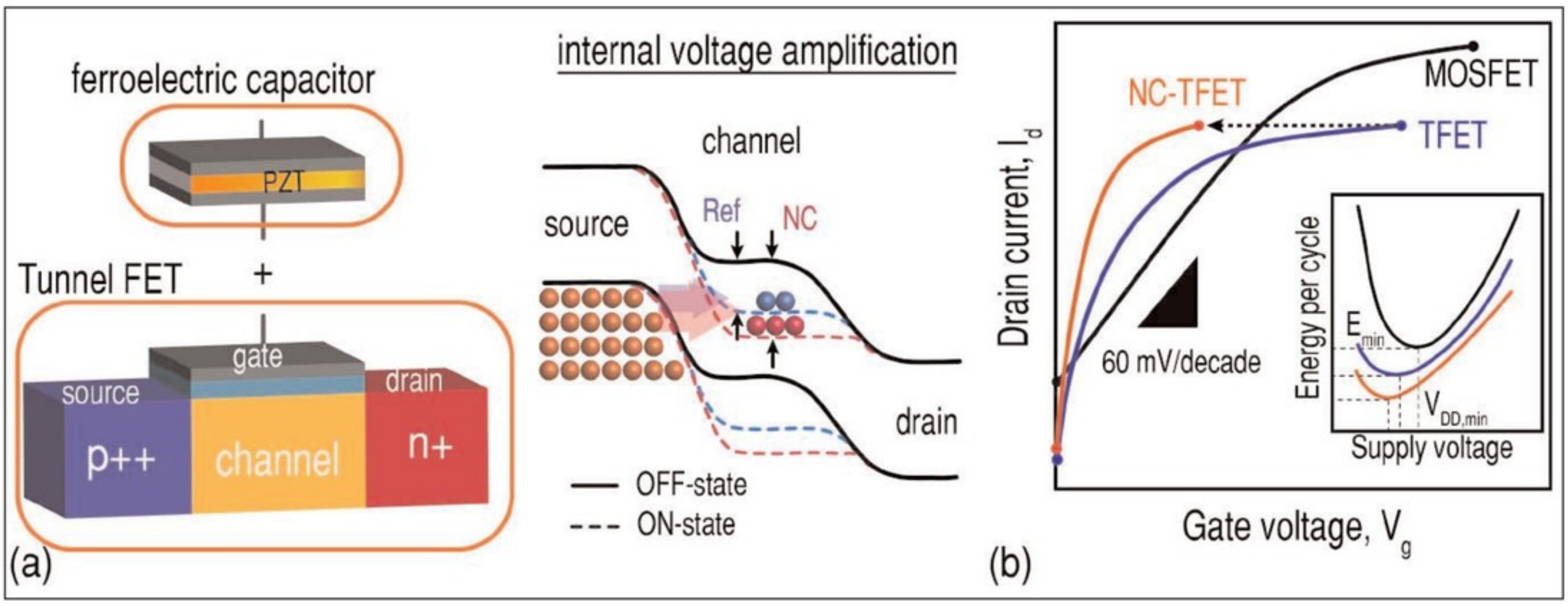

Figure 5. (a) Schematic of NC-TFET (left) combining ferroelectric capacitor with TFET gate. Series-connected NC booster amplifies gate voltage, increasing tunneling probability (right). (b) Drain current versus gate voltage plot and energy efficiency (inset) comparisons of MOSFET, TFET, and NC-TFET.

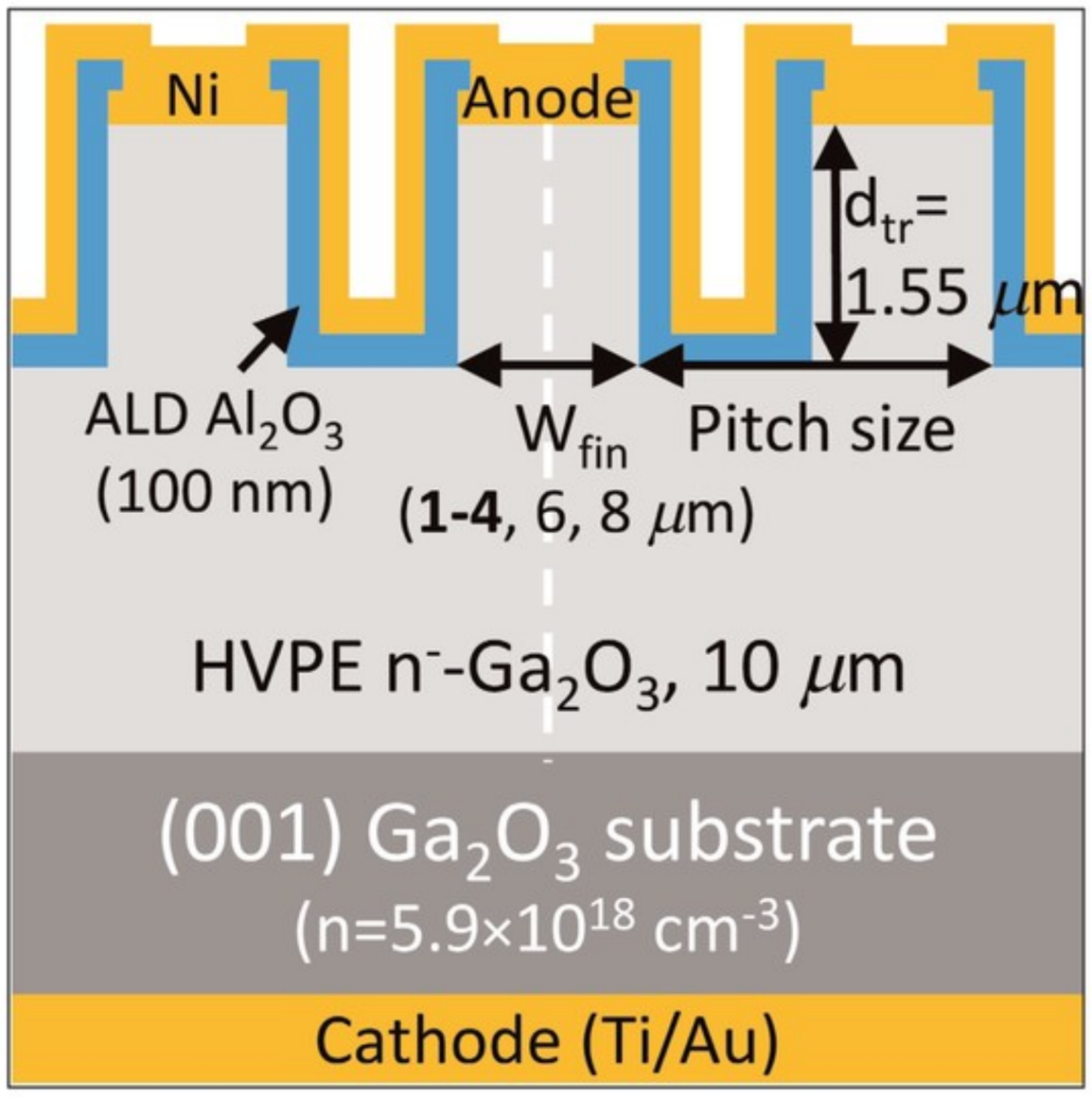

Figure 6. Schematic cross section of Ga_2O_3 trench SBDs.

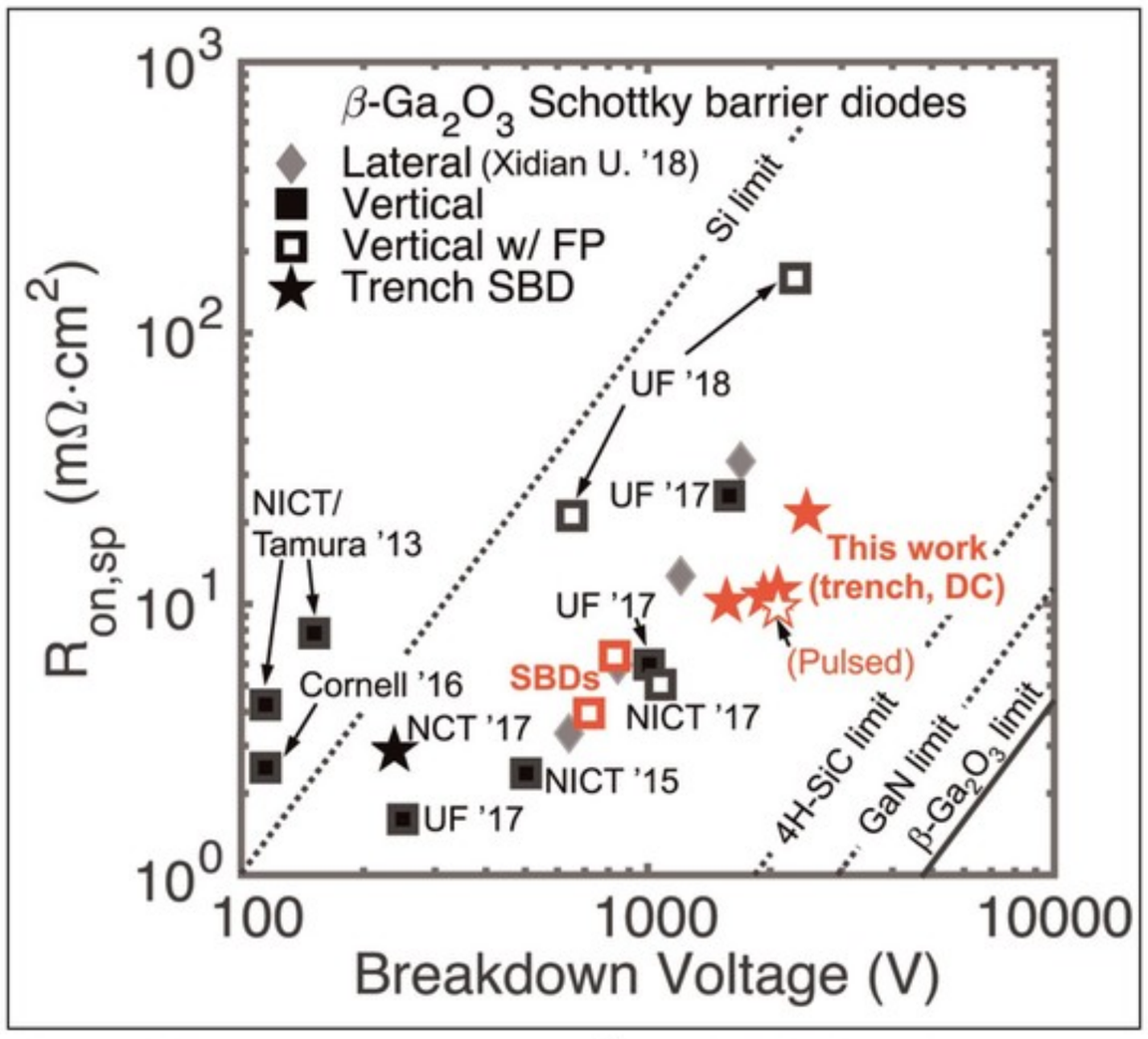

Figure 7. Benchmark plot of β-Ga_2O_3 SBDs: 1μm-trench SBD achieves highest BV, while the 2μm-trench SBD achieves the highest FOM, even without dedicated field-management techniques.

crowding. The back ohmic contact was titanium/gold (Ti/Au). Atomic layer deposition (ALD) aluminium oxide (Al_2O_3) insulated the trench sidewalls and bottoms. The Schottky contacts at the top of the fins consisted of nickel (Ni).

Devices with 1μm fin width achieved a record breakdown voltage of 2.44kV, according to the team. Simulations of devices with 2kV reverse bias gave a peak field with sharp 90° trench corners of ~5.9MV/cm. The rounding of the corners in the fabricated devices should mean the peak field was less than this.

A device with 2μm fin width and 2μm trench width gave the best Baliga figure of merit (FOM): 0.39GW/cm^2 under DC operation and 0.45GW/cm^2 using pulsed measurements. The Baliga FOM combines the breakdown voltage (BV) and specific on-resistance ($R_{on,sp}$) as BV^2/R_{on} (Figure 7).

Another effort aimed at Ga_2O_3 was the reported development of "the first self-consistent device (TCAD), circuit (HSPICE), and package (COMSOL) model considering [self-heating effects] which predicts FET performance on variety of substrates accurately" by Purdue University, USA [Session 24.6].

The Purdue team suggests on the basis of simulations that a template with a high thermal conductivity (400W/m-K) hexagonal boron nitride layer on sapphire for deposition of Ga_2O_3 could be one way to reduce self-heating in such devices.

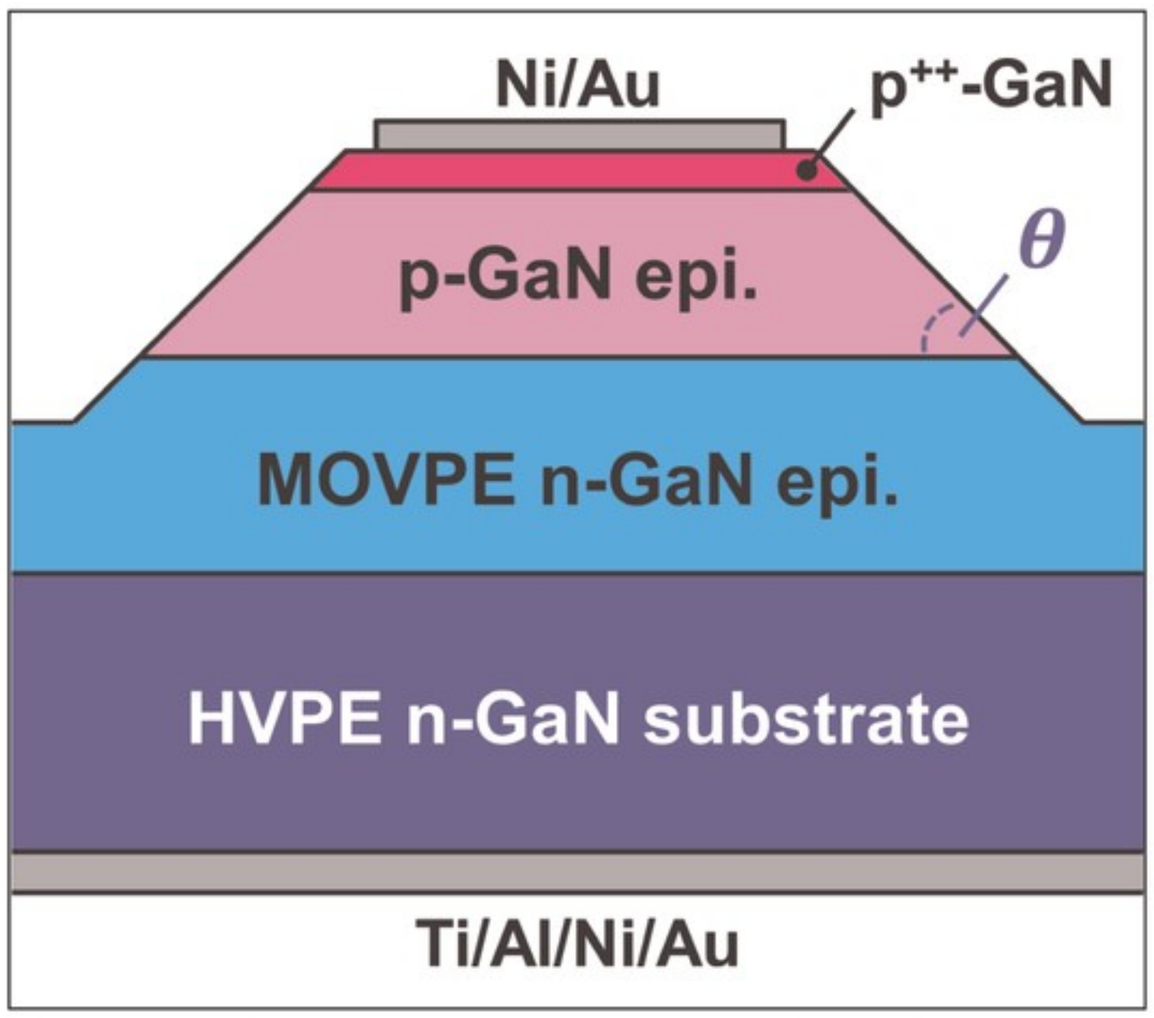

Figure 8. Schematic cross section of GaN PND with double-side-depleted shallow bevel termination. Angles were θ ~12°.

Gallium nitride

Kyoto University, Toyota Central R&D Labs Inc and Nagoya University in Japan reported novel bevel-mesa GaN pn diodes (Figure 8) with 2.8–3.5MV/cm parallel-plane breakdown electric fields "among the best of the reported non-punch-through GaN vertical devices" [Session 30.1].

The beveling was modified by the use of lightly doped p-GaN for which a growth technique has recently been developed with magnesium concentrations of order 10^{17}/cm^3. This allowed the depletion regions on the two sides of the junction to be balanced. The substrate was bulk GaN grown by hydride vapor phase epitaxy. The device layers were processed by metal-organic

vapor phase epitaxy. The researchers used growth conditions that avoided residual carbon incorporation, which can reduce doping effectiveness. The mesa angle (θ) was 12°. The mesa was created by inductively coupled plasma to a depth of 3.6μm.

The breakdown voltages of the devices depended on the thicknesses of the devices layers: 480V for 3.3μm p- and n-type layers, 180V for 1.5μm. The corresponding peak electric fields were calculated at 2.8MV/cm and 3.5MV/cm. The breakdown was not catastrophic, but occurred through avalanche, and the same characteristics could be reproduced repeatedly.

Hong Kong University of Science and Technology (HKUST) reported on the use of crystalline gallium oxynitride (GaON) channels to suppress hole-induced performance degradation in enhancement-mode metal-insulator-semiconductor FETs (MIS-FETs) [Session 30.3].

Hole-induced gate dielectric breakdown can shift threshold voltages of such devices, leading to instabilities and breakdown in performance. A GaON channel creates a hole-blocking ring in the gate region due to a valence band offset with respect to the neighboring GaN (Figure 9). The ring prevents holes attacking the gate dielectric.

The GaON was formed by oxygen exposure in an inductively coupled plasma (ICP) chamber after etching the gate recess. The material was annealed in ammonia in the low-pressure chemical vapor deposition (LPCVD) chamber used to create the silicon nitride passivation. The resulting GaON layer was 5.6nm and the bandgap was estimated at 4.1eV.

Negative-gate-bias stress tests resulted in significant threshold shifts in GaN-channel devices with the drain at 200V. This shifting was much reduced in the GaON MIS-FET. A further stress test with the gate at –20V relative to the source, and the drain at +320V relative to the gate, showed five-fold increased time to breakdown for the GaON-channel transistor, compared with a GaN channel.

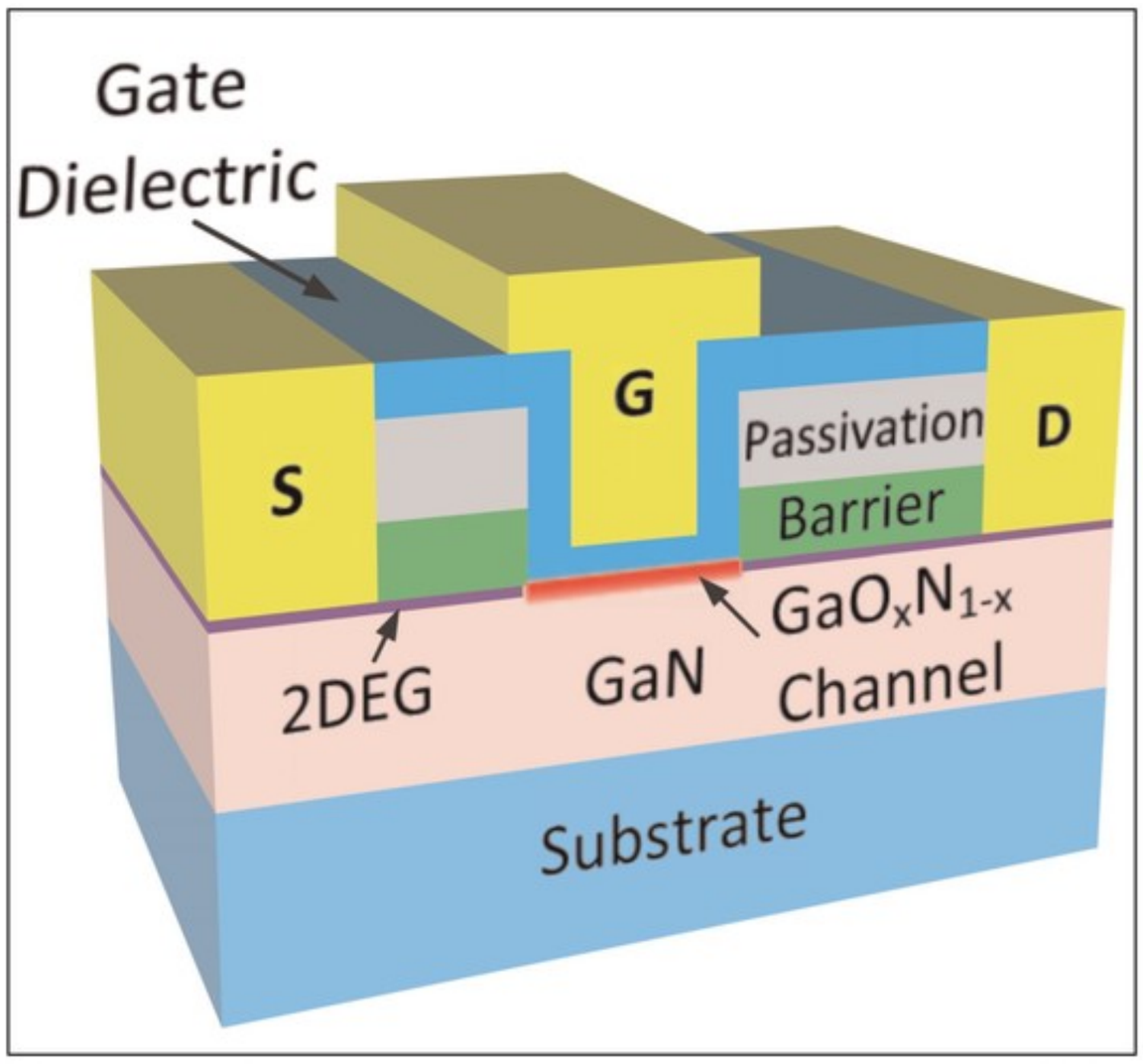

Figure 9. Schematic cross-sectional view of the MIS-FETs with recessed gate structure and GaON channel.

Silicon carbide

Japan's National Institute of Advanced Industrial Science and Technology (NAIST) claimed the lowest ever specific on-resistance ($R_{on,sp}$) for SiC-MOSFETs with a blocking voltage (B_v) of more than 600V [Session 8.1]. The researchers fabricated super-junction V-groove trench MOSFETs (SJ-VMOSFETs), with 0.63mΩ-cm^2 $R_{on,sp}$ and 1170V B_v.

The researchers report: "We have improved drastically the trade-off relationship between on-resistance and the breakdown voltage by narrowing SJ cell pitches and higher doping concentration in SJ regions. In addition, we have reduced the parasitic resistance by a thin V-groove {0$\bar{3}$3$\bar{8}$} channel."

Super-junction devices use vertical pillars of alternately doped regions, allowing better control of current flow between the source and drain electrodes with reduced on-resistance (Figure 10). The pillars were

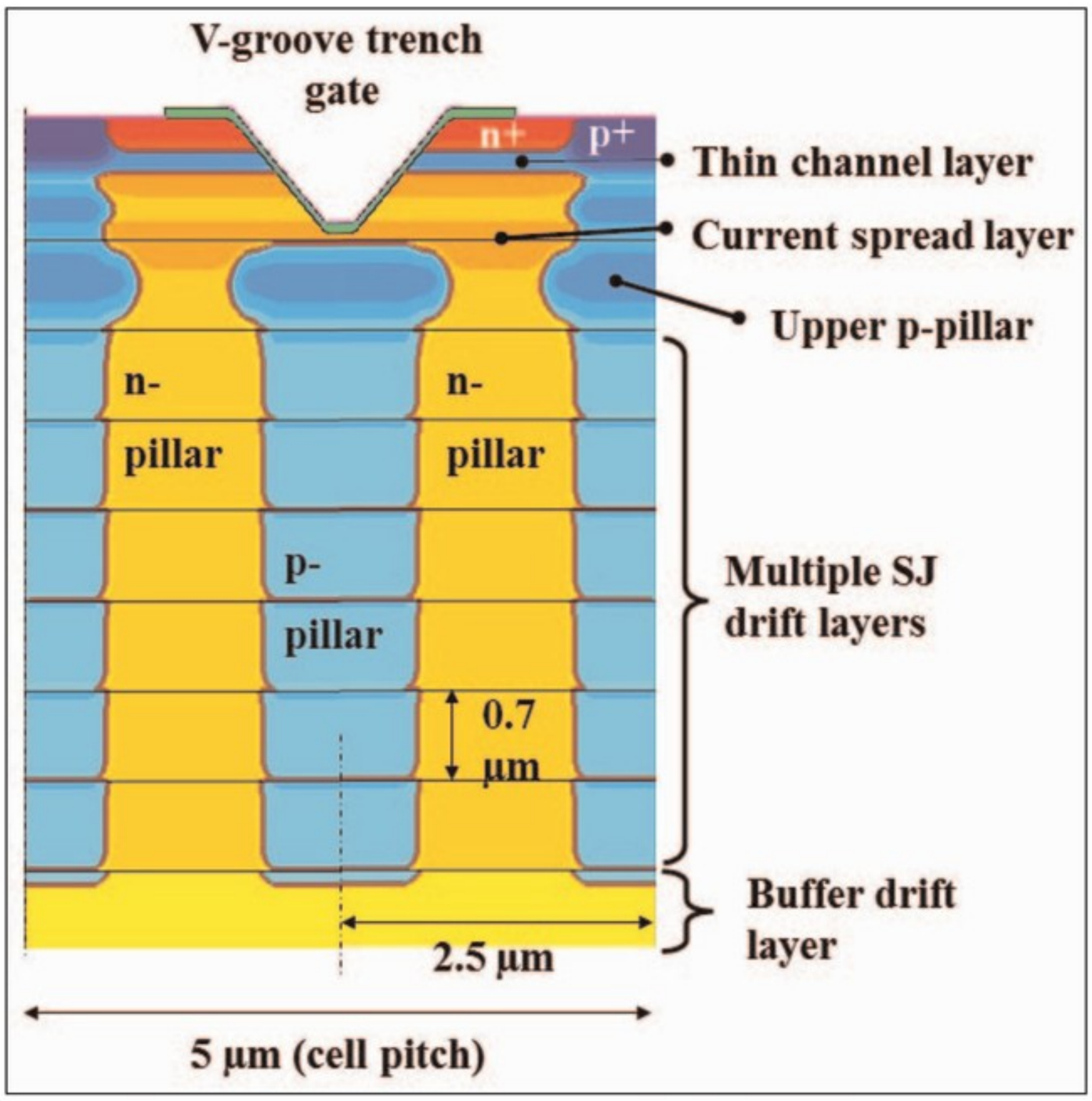

Figure 10. Schematic cross section of SJ-VMOSFET.

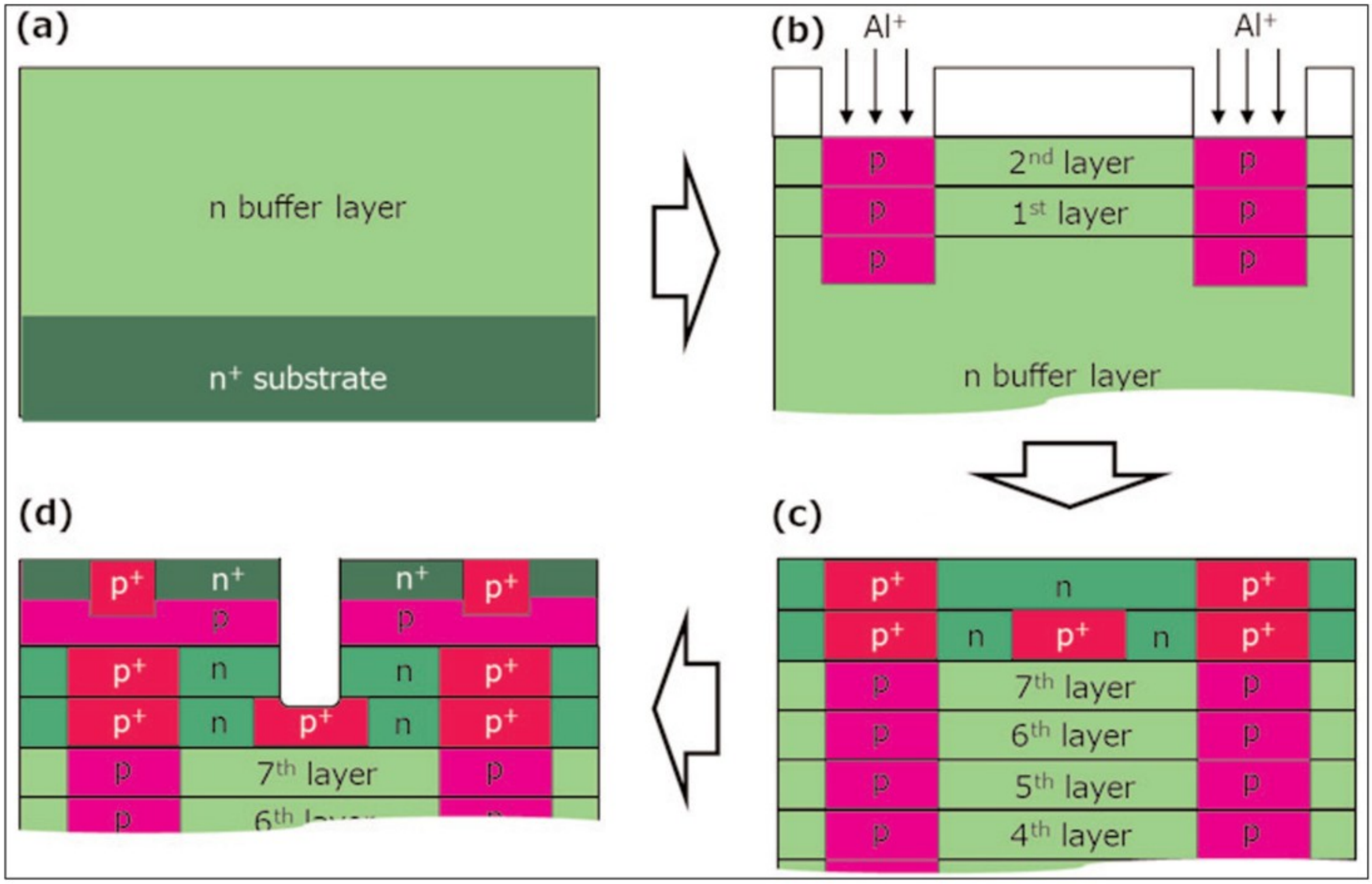

Figure 11. Fabrication flow of SiC SJ-UMOSFET through multi-epitaxial growth method.

formed by a sequence of six epitaxial growth and aluminium ion implantation steps for the n- and p-type regions, respectively.

Another group at NAIST presented 1.2kV-class U-shape trench gate MOSFETs using a similar super-junction structure produced in seven epitaxial and Al ion implantation steps [Session 8.2]. The alignment accuracy of the multi-step process (Figure 11) is reported as being within 0.1μm.

Researchers at Mitsubishi Electric Corp and University of Tokyo in Japan have found that using sulfur (S) as a deep-level donor in 4H-SiC MOSFETs (Figure 12) enables a 31% reduction of specific on-resistance with high 4.0V threshold voltage [Session 8.3]. The resistance reduction was measured in a vertical MOSFET relative to a device without sulfur doping.

These findings run counter to the general belief that deep-level donors are not suitable for high-performance electronics. The researchers' simulations suggest that the improved threshold is due to the increased ionization energy of the sulfur. At the same time, the sulfur doping improves inversion layer mobility in the channel.

The experiments were claimed as the first time that sulfur was used for donor doping in the channel region of 4H-SiC MOSFETs. Both lateral and vertical devices were fabricated. The S atoms were introduced by ion implantation. The gate insulator was formed by thermal oxidation and was subsequently subjected to nitridation in diluted nitric oxide (NO). ■

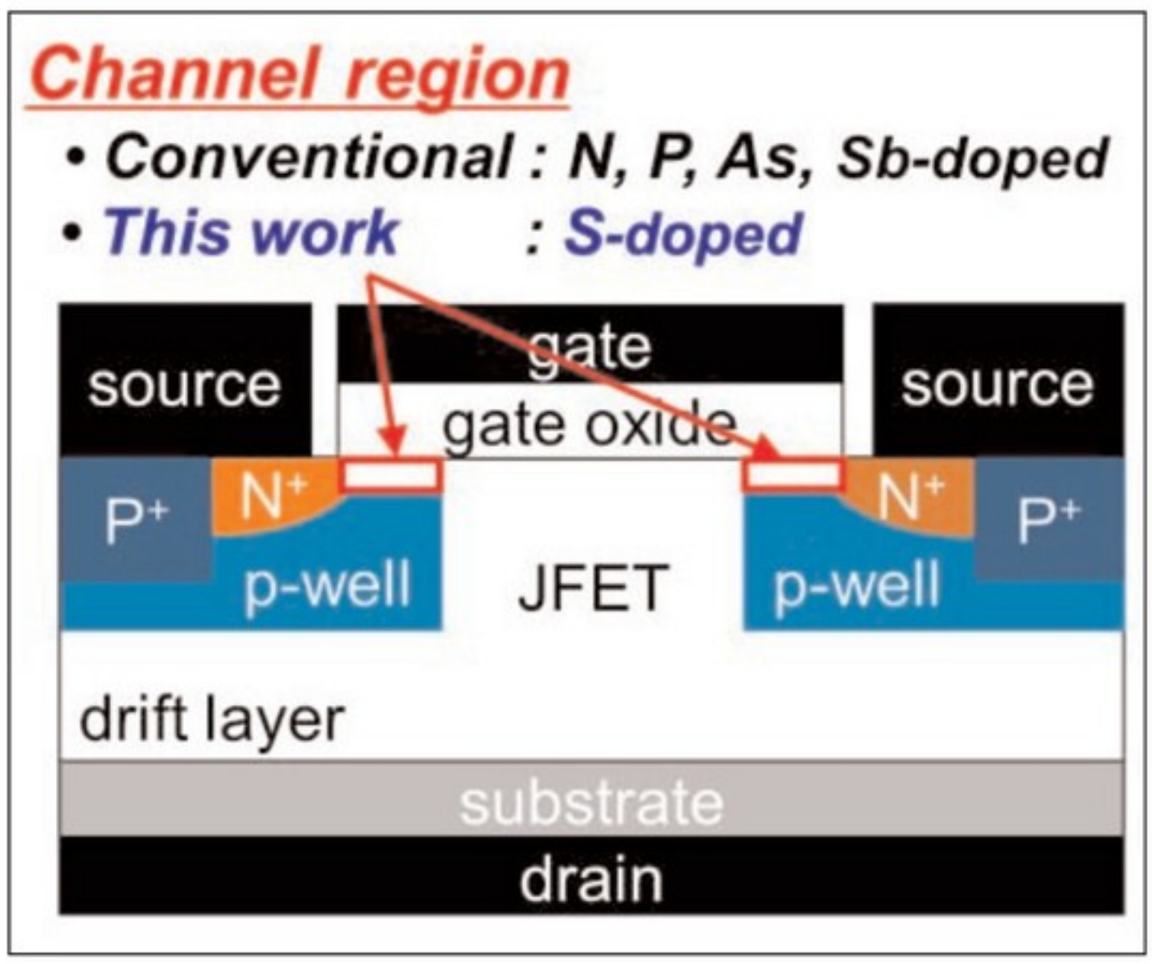

Figure 12. Schematic cross section of vertical 4H-SiC MOSFETs with S-doped channel region.

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